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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,001	07/08/2003	Shibly S. Ahmed	H1484	6254

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,001	AHMED ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *9-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 14-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/8/3
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Restriction/Election

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-8 and 14-20, drawn to a semiconductor device, classified in class 257, subclass 412.

   II. Claims 9-13, drawn to a method of making semiconductor devices, classified in class 438, subclass 1+.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the Group I invention could be made by a materially different process, for example, by forming a fully silicided gate without first partially siliciding the gate.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Glenn Snyder (Reg. No. 41,428) on March 11, 2001, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-8 and 14-20. Affirmation of this election must be made by applicant in replying to this

Office action. Claims 9-13 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

6. Claims 1-8, 14-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fried et al. (U.S. Patent No. 6,657,259 B2) in view of Wang et al. (U.S. Patent No. 6,589,836 B1).

In re claim 1, Fried (Fig. 7b) discloses a semiconductor device, comprising:

A substrate (202);

An insulating layer (204) formed on the substrate;

A first device formed on the insulating layer, including:

A first fin (206) formed on the insulating layer, and

A first silicided gate (212; column 10, lines 7-8) formed over a portion of the first fin and including a first thickness of silicide material; and

A second device formed on the insulating layerr, including:

A second fin (206) formed on the insulating layer, and

A second silicided gate (212) formed over a portion of the second fin and including a second thickness of silicide material.

Fried discloses a layer of silicide (212) atop the gate regions but does not expressly disclose the silicide regions over each gate region comprising a separate silicide thickness. Wang (Fig. 7) discloses thin (15b) and thick (15c) silicide layers atop gate structures (6). It would have been obvious for one skilled in the art at the time of the invention to use replace the uniform thickness silicide layers of Fried with the dual thickness silicide layers disclosed by Wang for the purpose, for example, of diversifying the device by varying the resistance of the gate layers (Wang; column 4, lines 54-57).

In re claim 2, Fried in view of Wang discloses the device of claim 1, further comprising:

A first dielectric layer (Fried, 208; column 8, lines 1-6) formed between the first fin and the first silicide gate and wherein the second device further includes:

A second dielectric layer (Fried, 208) formed between the second fin and the second silicided gate.

In re claim 3, Fried in view of Wang discloses the device of claim 1, wherein the first silicide gate is partially silicided and the first thickness ranges from about 100 to 500 angstroms (Wang; column 4, lines 60-63).

In re claim 4, Fried in view of Wang discloses the device of claim 1, wherein the second silicided gate is fully silicided.

In re claim 5, Fried in view of Wang discloses the device of claim 4, wherein the second thickness ranges from about 400 to 1000 angstroms (Wang; column 4, lines 50-54).

In re claim 6, Fried in view of Wang discloses the device of claim 1, wherein the first device is a NMOS device and the second device is a PMOS device (Fried, column 8, lines 1-30; Wang; column 4, lines 50-63).

In re claim 7, Fried (Fig. 8) in view of Wang discloses the device of claim 1, wherein the first device and the second device are included in a single circuit element (Fried; column 11, lines 64-67; column 12, lines 1-8).

In re claim 8, Fried in view of Wang discloses the device of claim 1, wherein a first threshold voltage of the first device is lower than a second threshold voltage of the second device (as understood by Applicant's Disclosure, section [0050], silicide layers of varying thicknesses inherently have varying threshold voltages.)

In re claim 14, Fried (Fig. 7b) discloses a semiconductor device, comprising:

A substrate (202);

An insulating layer (204) formed on the substrate;

A first device formed on the insulating layer, including:

A first fin (206) formed on the insulating layer,

A first dielectric layer (208; column 8, lines 1-6) formed on the first fin, and

A silicided gate (212) formed over a portion of the first find and the first dielectric layer; and

A second device formed on the insulating layer, including:

A second fin (206) formed on the insulating layer,

A second dielectric layer (208) formed on the second fin, and

A silicided gate (212) formed over a portion of the second fin and the second dielectric layer.

Fried discloses a layer of silicide (212) atop the gate regions but does not expressly disclose the silicide regions over each gate region comprising a separate silicide thickness. Wang (Fig. 7) discloses thin (15b) and thick (15c) silicide layers atop gate structures (6). It would have been obvious for one skilled in the art at the time of the invention to use replace the uniform thickness silicide layers of Fried with the dual thickness silicide layers disclosed by Wang for the purpose, for example, of diversifying the device by varying the resistance of the gate layers (Wang; column 4, lines 54-57).

In re claim 15, Fried in view of Wang discloses the device of claim 14, wherein the first silicide gate is partially silicided and the first thickness ranges from about 100 to 500 angstroms (Wang; column 4, lines 60-63).

In re claim 16, Fried in view of Wang discloses the device of claim **14**, wherein the second thickness ranges from about 400 to 1000 angstroms (Wang; column 4, lines 50-54).

In re claim 17, Fried in view of Wang discloses the device of claim 14, wherein the first device is a NMOS device and the second device is a PMOS device (Fried, column 8, lines 1-30; Wang; column 4, lines 50-63).

In re claim 18, Fried (Fig. 8) in view of Wang discloses the device of claim 14, wherein the first device and the second device are electrically connected (Fried; column 11, lines 64-67; column 12, lines 1-8).

In re claim 20, Fried in view of Wang discloses the device of claim 14, wherein a first threshold voltage of the first device is lower than a second threshold voltage of the second device

(as understood by Applicant's Disclosure, section [0050], silicide layers of varying thicknesses inherently have varying threshold voltages.)

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fried in view of Wang as applied to claim14 above, and further in view of Takeda et al. (US 2001/0045589 A1).

In re claim 19, Fried in view of Wang discloses the device of claim 14, but does not expressly disclose a third FET with a third thickness of a silicide region atop the gate. Devices with three FETs overlaid by silicide are well known in the art (Takeda, Fig. 3). It would have been obvious for one skilled in the art at the time of the invention to provide a third FINFET device disclosed in the manner of Fried with a third thickness of silicide as disclosed by Wang for the purpose, for example, of further diversifying the capabilities of the semiconductor device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815